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INTEGRATED FIBER-OPTIC COUPLER BY: PR PRUCNAL, ER LOSSUM

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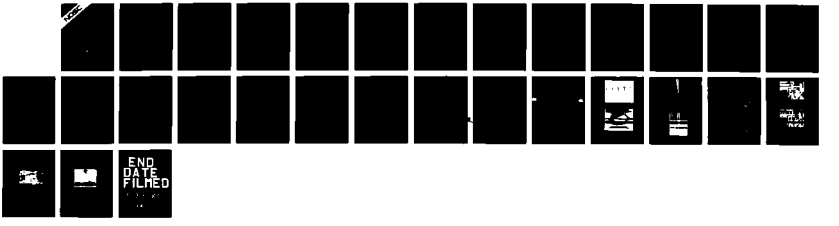

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NAVAL OCEAN SYSTEMS CENTER San Diego, California 92152-5000

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Integrated Fiber-Optic Coupler

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This report describes a silicon photodetector structure exhibiting real-estate efficient coupling of optical fibers to semiconductors. The integrated fiber-optic coupler employs a vertical insertion of a tapered single-mode fiber into a laser-etched cylindrical hole in a semiconductor substrate. It features a small surface footprint, mechanical stability, and accurate alignment. The p-n junction detectors have typically shown responsivities of 0.23 A/W at 0.63 μm, corresponding to a quantum efficiency of 45 percent, and dark currents below 1 nA.

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INTEGRATED FIBER OPTIC COUPLER

Abstract

This report summarizes the research carried out during the first year of support under this program. A silicon photodetector structure exhibiting real-estate efficient coupling of optical fibers to semiconductor devices is described. The integrated fiber optic coupler employs vertical insertion of a tapered single-mode fiber into a laser-etched cylindrical hole in a semiconductor substrate. It features a small surface footprint, mechanical stability, and accurate alignment. The p-n junction detectors have typically shown responsivities of 0.23 A/W at 0.63 um, corresponding to a quantum efficiency of 45 %, and dark currents below 1 nA.

I. INTRODUCTION

This report covers the first year of support for investigating the integrated fiber optic coupler (IFOC) concept. In the IFOC structure, the tip of a tapered optical fiber is inserted into a cavity which has been formed in a semiconductor. A photodetector or photoemitter device structure is fabricated in, or adjacent to, the cavity so that light is coupled between the fiber and device. The resultant structure features a small surface footprint and mechanical stability with accurate alignment, thus making it ideally suited for optical interconnects between integrated circuits.

In this first year of support, we have designed, fabricated, and characterized a silicon photodetector IFOC device (Fig. 1). The p-n junction device was fabricated in a laser-etched cavity 15 um in diameter and 20 um deep on the front surface of a silicon integrated circuit chip. The IFOC responsivity is approximately 0.23 A/W at 0.63 um wavelength (the quantum efficiency is 45 %) and has a dark current below 1 nA. The device characteristics, although sufficient for many applications, can most likely be improved further through design and fabrication process modification.

The report will summarize the progress made during the first year of support and then discuss the present fabrication process and device characteristics. Finally, plans for the second year will be addressed.

There appears to be a high degree of interest in the industrial

community in this research. Several papers have been given at conferences in the past year, and we have published one letter. A longer paper has been submitted to the IEEE Transactions on Electron Devices journal for publication.

II. BACKGROUND

The use of optical interconnections between high speed integrated circuits is viewed as a potential solution to a growing problem in VLSI technology. Conventional metallic conductors, carrying electronic signals from chip to chip, are susceptible to electromagnetic coupling which can result in parasitic capacitance, inductance, and noise pick-up. Overall system performance, particularly at high bit rates, suffers from the limitations thus imposed by the interconnections. Signals transmitted photonically are immune to these effects, and this accounts for much of the current interest in optical interconnection. Potential applications of optical interconnects have been evaluated theoretically; skewless distribution of clock signals and routing of chip-to-chip data links via optical fibers are among those considered promising [1,2]. These applications would require a means of coupling a large number of fibers to a single semiconductor chip, but no standard technique to satisfactorily perform this function now exists. Techniques employing lens elements [3], a Burrus-type structure [4], or simple butt-coupling [5], which have been used for coupling fibers to discrete optoelectronic components, require too much space to be useful in VLSI interconnection schemes. A recently reported hybrid approach [6], using silicon V-grooves to guide fibers into an integrated 12 x 1 photodiode array, would place restrictions on

detector placement as well as presenting assembly and stability problems typically associated with hybridization. The most technically advanced technique reported to date employs a horizontal fiber terminating in an angled, mirrored facet which reflects incoming light down onto the semiconductor substrate [7]. However, use of a multi-mode fiber requires a large area detector, and the lateral approach consumes considerable on-chip real estate, limiting the number of fibers that may be coupled to a single IC chip.

III. PROGRESS SUMMARY

The progress can be broadly divided into four major efforts: cavity formation, detector fabrication, fiber preparation, and fiber insertion. These efforts proceeded in parallel so that although an IFOC device was demonstrated early in the program, the performance of the subsequent devices has improved steadily as each area of effort yields results. The IFOC devices have been fabricated using patterns on previously existing masks, and incorporated into charge-coupled device circuits.

Cavity formation has taken place predominantly by a laser assisted etching process under the direction of Prof. Osgood. During the year, the etching parameters have been established so that the cavities can be made reproducibly in a controlled manner. An effort was also made to utilize anisotropic crystallographic etching (Fig. 2a) since the process promised easy fabrication without the damage associated with reactive ion etching. However, for small geometry cavities, it is difficult to insure proper crystallographic alignment (see Fig. 2b).

At the present time, laser-assisted etching remains the preferred method for fabricating the cavities.

Detector fabrication has focused on reducing both dark current and series resistance in the p-n junctions. Solid state diffusion from both spin-on and solid sources has been investigated. At the present time, with the proper process modifications, the techniques seem equally reliable.

Fiber preparation has also proceeded well. Initially, fiber tapering was achieved using a melt and pull technique. In this case, both the cladding and core were reduced in diameter over a significant length of fiber (Fig. 3a). A chemical etching technique which yields a conical shape (Fig. 3b) is now the preferred method for fiber tapering, both in terms of optical losses and mechanical integrity.

Reliable insertion of the optical fiber into the IFOC cavity has been achieved by developing a dedicated work station which includes both visual and optoelectronic monitoring of the insertion process. A method of affixing the fiber to the IFOC, which does not require the application of epoxy to the integrated circuit surface, has been developed.

IV. DEVICE FABRICATION

The fabrication of the IFOC device proceeds in two distinct stages: the formation of the detector, and the preparation and insertion of the optical fiber. In the first stage, a 10 Ω-cm n-type silicon wafer with (100) orientation is cleaned and oxidized in steam at 900 °C. Photolithography is performed to define alignment marks in the substrate and to open windows for the

etching of the detector cavities, which is done using a non-thermal, laser-induced wet etching technique [9]. Typically, the silicon substrate is covered with a dilute HF solution (10% by volume in DI water) and a continuous wave UV beam is focused onto the substrate at the desired location. The UV beam is obtained from a frequency doubled argon ion laser yielding a 257 nm line. The power density of the illuminating spot determines the etch rate, and the spot size determines the final hole diameter, which is between 15 and 18 um for the work described here. A 20 minute etch at a power density of 10 W/cm^2 is used to form the 20-25 um deep cylindrical holes which serve as coupling sites in the IFOC structure. The technique allows for holes of any depth to be drilled while maintaining vertical sidewalls with no significant variation in diameter, since light-guiding within the cavity for deep UV wavelengths results in a highly anisotropic etch. This characteristic, as well as the non-thermal, damage-free nature of the process, makes the laser-assisted etching technique most advisable for the creation of cavities which will serve as active circuit elements. Laser radiation can also be used to thermally etch holes, but damage induced on the surrounding area is considerable and undesirable. Adverse effects arising from substrate damage, such as increased dark current and trap-related noise, were major considerations in ruling out the use of reactive ion etching for detector cavity formation. Anisotropic wet etching techniques, which yield crystallographically defined vertical-walled trenches in (110) oriented substrates [10], were found to be unsuitable for applications requiring three-dimensional features with more than one set of vertical walls [11].

Although the laser-assisted etching process is currently performed serially, its throughput can be increased by switching to a projection etching process using an excimer laser [12].

After etching, the remaining oxide is stripped and a 5000 A thick field oxide is grown in steam at 900 °C. A diffusion window centered on the etched hole is opened and dopant is introduced by one of two techniques. One alternative involves the use of a boron-containing polymer spin-on film to dope the exposed silicon, including the inner surface of the hole. An analysis of spin-on doping of similar structures [13] indicates that predeposition is assisted by capillary action for holes with aspect ratio less than five, as used in the IFOC. However, to experimentally determine whether gas phase predeposition of dopant might be better suited to the cavity geometry, use of a solid diffusion source was also investigated. Reproducible and consistent results were obtained with both techniques, and they are considered to be equally viable for this application. Following predeposition, a 110 minute impurity drive-in is performed at approximately 1000 °C in an open-tube furnace with a 95% N_2/5% O_2 gas mixture flowing.

Following the diffusion of the detector cavity, a window for contacting the detector is opened and 3000 A of aluminum is evaporated and patterned photolithographically. The most important aspect of this step is the removal (by a standard wet etch) of all aluminum from the cavity's interior, decreasing optical loss due to reflections. Finally, a backside aluminum contact is evaporated, followed by a twelve minute forming gas anneal at 400 °C. As the above description implies, IFOC device fabrication is compatible with

standard integrated circuit processing. We have recently fabricated a charge-coupled device test chip configured to accept both electronic and fiber optic inputs. Ongoing tests indicate that the inclusion of IFOC sites has no detrimental effect on adjacent circuitry.

The second stage of fabrication begins with the preparation of the optical fiber. The tip of a single-mode Corning fiber with a core diameter of 9 um and a cladding outer diameter of 125 um is tapered to approximately 12 um in a continuously stirred solution of HF buffered with ammonium fluoride. In order to obtain the desired profile, a portion of the fiber's plastic jacket (which resists the HF etch) is removed and then the length of exposed glass is reduced to about 40 um using a straight-pull scribe and break technique [14]. Inhibited transport of etchant inside the jacket results in a conically tapered profile with a half-angle of 12-15 degrees. Since the distance that must be etched radially (55 um) is greater than the length of exposed glass, the tip lies within the protective jacket at the conclusion of the three-hour etch. This facilitates safe storage of the batch-fabricated fibers prior to the final assembly of the device. The final assembly step involves mechanically stripping back the jacket, carefully inserting the fiber into the detector cavity, and fixing it with respect to the microcircuit package that houses the IFOC chip. The insertion process is performed on a dedicated work station, which is drawn schematically in Fig. 4.

The insertion station consists of a mount for the circuit package, an X-Y-Z translational stage with a vacuum chuck fitting

to hold the optical fiber, and an Olympus SZH microscope which gives reasonable magnification while maintaining a long focal length for maximum working distance. The microscope is angled 45 degrees from both the fiber and the chip, affording a clear view to aid the operator in achieving proper mechanical mating. Electrical connection is made to the photodiode through the mounting box, and live photocurrent monitoring supplements visual observation in the determination of the best final resting position for the fiber. Fig. 5 shows two photographs taken through the microscope during the insertion process. Following insertion, the fiber tip remains in place despite small movements of the vacuum chuck, indicating the lateral alignment stability provided by the etched hole.

To prevent stress on the taper, a UV-cured adhesive is used to affix the fiber to the edge of a glass slide bonded onto the microcircuit package. This is done at a point approximately 300 um above the chip surface, where both the cladding and the protective jacket of the fiber are still intact. No adhesive is needed at the surface of the chip, as in other fiber-optic coupler designs [4-7], because the detector cavity itself prevents any lateral misalignment. The package configuration is stable enough that no fiber has yet pulled out of a detector cavity during testing once it has been bonded to the slide. Adhesion at the fiber-slide joint and physical mating between the vertically-inserted fiber and the cavity combine to ensure a stable, well-aligned structure. This reveals one advantage inherent in the use of vertical coupling structures for optical interconnect applications. Furthermore, as the level of integration in VLSI circuitry increases, Rent's rule [1]

predicts that the required number of interconnections will outpace the availability of connection sites on the chip periphery. This "pinout problem" is best addressed by providing interconnection sites in the chip's interior; the vertical structure of the IFOC makes such an approach possible. A photograph demonstrating this appears in Fig. 6. The fiber-to-fiber spacing of ~1.5 mm seen there is determined by the pre-existing chip layout. Simulations of the packaging process, involving the insertion and bonding of tapered fibers into holes etched in unprocessed silicon chips, have achieved fiber spacings as low as 300 um, limited primarily by the bulky adhesive layer applied to the edge of the glass slide. It is likely that more sophisticated packaging techniques will permit IFOC arrays with center-to-center spacing nearly as small as the outer cladding diameter of the fibers used.

V. DEVICE CHARACTERIZATION

Electrical characterization of the photodetectors included measurement of series resistance, capacitance, and dark current, both before and after device packaging. Information concerning the quality of the fabrication process, particularly the effects of steps unique to the process, can be obtained from this data, which is also gathered for test structures on adjacent sites. The average value for sheet resistance measured on diffused test sites was 25 Ω/□, predicting a series resistance for the IFOC photodiode geometry of R_S = 25Ω. This is in accord with experimental values of 50-80 Ω for fabricated devices, if contact resistance effects are included. The capacitance and dark current of the reverse

biased photodiodes are recorded in a sweep from 0 to -10V. Typically, a junction capacitance of 10 pF at -5V was noted for unpackaged diodes, with an additional 2-3 pF due to bond wires and instrumentation interfaces seen after packaging.

Measurement of the dark current of IFOC photodiodes and comparison with that of adjacent test diodes provided the primary quality control data for the overall process. Devices exhibiting soft low-voltage breakdown (V_B = 3-10 V), or dark current greater than an arbitrary cutoff value of 2 nA at -10V were considered failures, and they comprised about half of the fabricated IFOCs. This was only slightly greater than the "failure" rate of test diodes with identical areas, excluding the etched cavity. The difference is believed to be due primarily to the greater difficulties of removing chemical contaminants from the inside of the etched holes. Several fabrication runs employing especially thorough cleaning processes yielded devices with a reduced incidence of failure. On occasion, increases in the photodiode dark current were observed while monitoring the device's I-V characteristic during the fiber insertion process. This effect appeared in very few instances, and generally in conjunction with breakage of the tapered fiber tip inside the cavity. Occurrences of this sort are easily detected and avoided, and couplers with properly seated fibers show no dark current anomalies. However, such effects should be carefully monitored during long-term device operation. Overall, it was normal processing considerations, rather than those related to IFOC fabrication, that set the limits on device performance and yield.

From the average values of series resistance (R_S) and junction

capacitance (C_j) obtained, a diode cutoff frequency $f_t = (2\pi R_s C_j)^{-1} = 200$ MHz could be inferred. This would be realized in a p-i-n diode with these parameters, but carrier diffusion delays in the current p-n structure further limit the operating speed. Since high speed performance of the devices in the next design iteration should be RC-limited, it is important to determine the extent to which these values may be reduced. A decrease in capacitance by a factor of 10 can be achieved without altering the basic IFOC design, simply by eliminating most of the excess p-n junction area surrounding the cavity. Additionally, a reduction in series resistance is expected to result from more comprehensive design alterations now being implemented. The relatively large value of R_s can be attributed to the unique geometry of the photodiode, which requires carriers generated at the bottom of the hole to drift the entire length of the cavity sidewalls before being collected at the upper contact. A structure allowing for ohmic contact to more of the active region would reduce R_s, but it must be configured so as to minimize optical loss due to reflections. A backside-illuminated photodetector structure which satisfies these criteria is currently under investigation, and will be described below.

Measurements employing a free-space He-Ne laser beam served to spatially profile the diode responsivity and to obtain values independent of any optical losses from the fiber. The observed uniformity of the photogenerated current, including instances in which the laser spot is focused entirely within the cavity, provided further confirmation of the success of the detector doping processes. Visual observation of this experiment revealed an additional

benefit of the detector geometry: while reflections were noted from surfaces surrounding the hole, a beam incident on its interior appeared to be completely absorbed. The average value of responsivity recorded in these measurements was 0.23 A/W, corresponding to a quantum efficiency of 45% for λ = 633 nm.

For measurement of net DC responsivity at 633 nm, the He-Ne laser beam was coupled into a single mode fiber which was spliced to the tapered IFOC fiber using a low-loss GTE laboratory splice. A curve tracer was used to monitor the I-V characteristic of the photodiode under illumination and in the dark. The difference between the two curves is the photogenerated current, I_{ph}, which was recorded at a 5V reverse bias. A sample datum is shown in Fig. 7.

VI. DISCUSSION AND FUTURE PLANS

The cavity approach advocated in the IFOC concept facilitates reliable and high-density direct connection of optical fibers to integrated circuits. Vertical connections have the advantage over lateral connections in that one is not constrained to the perimeter of the chip while maintaining minimal real-estate consumption. However, it is felt that back-side connections are preferred over the front-side prototype device described above. There are several reasons for this. First, in the front-side approach, the detector/emitter device is necessarily located below the plane of the surface circuitry and a low resistance vertical connection to the surface is required. Second, the fabrication of an optimal detector at the bottom of the cavity is difficult. Third, isolation of the detector from surface circuitry and adjacent detectors to prevent

minority carrier cross-talk and latch-up is difficult at IFOC cavity depths. Back-side connection, on the other hand, (provided the etching can be accurately controlled to stop a few microns from the front surface) eliminates all three of these difficulties.

Direct connection of optical fibers to silicon integrated circuits for receiver applications has been demonstrated. However, silicon is a poor material in which to build efficient emitter structures. Direct band-gap semiconductors such as binary and ternary compounds are preferred opto-electronic integrated circuit materials. Assuming that silicon continues to be the dominant material used in electronic circuits, then the widespread use of optical fiber interconnections may depend on hybrid approaches. For example, the growth of direct-band-gap materials on silicon [16,17] may be one solution. Another possibility is to form IFOC devices on direct band gap material (either individually, or as an array) and then hybridize such an IFOC "optical ribbon" connector onto the silicon chip, perhaps using solder bump technology. The advantage to this latter approach is that manufacturing yields of the III-V material IFOC and the silicon integrated circuit are decoupled.

Other technological hurdles yet to be solved in order to make optical interconnections economically viable for general application (but not part of this program) include an ability to daisy-chain connections (e.g., a low-loss optical tap), and an ability for optical signals to turn small curvature radii corners with low loss (e.g., a micro-mirror right angle fiber).

Although not a hurdle, a technique for fully utilizing the

terahertz bandwidth pctential of optical fibers when dealing with the gigahertz bandwidth of the fastest electronic integrated circuits would also be particularly useful. For example, two circuit boards which need several hundred interconnections, each with a 1 GHz bandwidth, might be interconnected with one optical fiber with a THz bandwidth if an appropriate, economical, multiplexing scheme could be devised. (This last discussion item has been added as food for thought, although Prof. Prucnal is currently investigating similar avenues under other support.)

VIII. PUBLICATIONS

1. P.R. Prucnal, E.R. Fossum, R.M. Osgood, "Integrated fiber-optic coupler for very large scale integration interconnects," Optics Letters, vol. 11, p. 109, 1986.

IX. CONFERENCE PAPERS

1. P.R. Prucnal, E.R. Fossum, R.M. Osgood, "Integrated fiber-optic coupler for very large scale integration interconnects," presented at J. Opt. Soc. 1985 Annual Meeting, Washington, D.C.

2. P.R. Prucnal, E.R. Fossum, R.M. Osgood, "Integrated fiber-optic coupler for VHSIC/VLSI interconnects," presented at Workshop on Optical Interconnects, MCC, Austin, Texas.

3. P.R. Prucnal, E.R. Fossum, R.M. Osgood, "Fiber-optic coupler for VHSIC/VLSI interconnects," presented at SPIE Annual Meeting, January 1986, Los Angeles, California.

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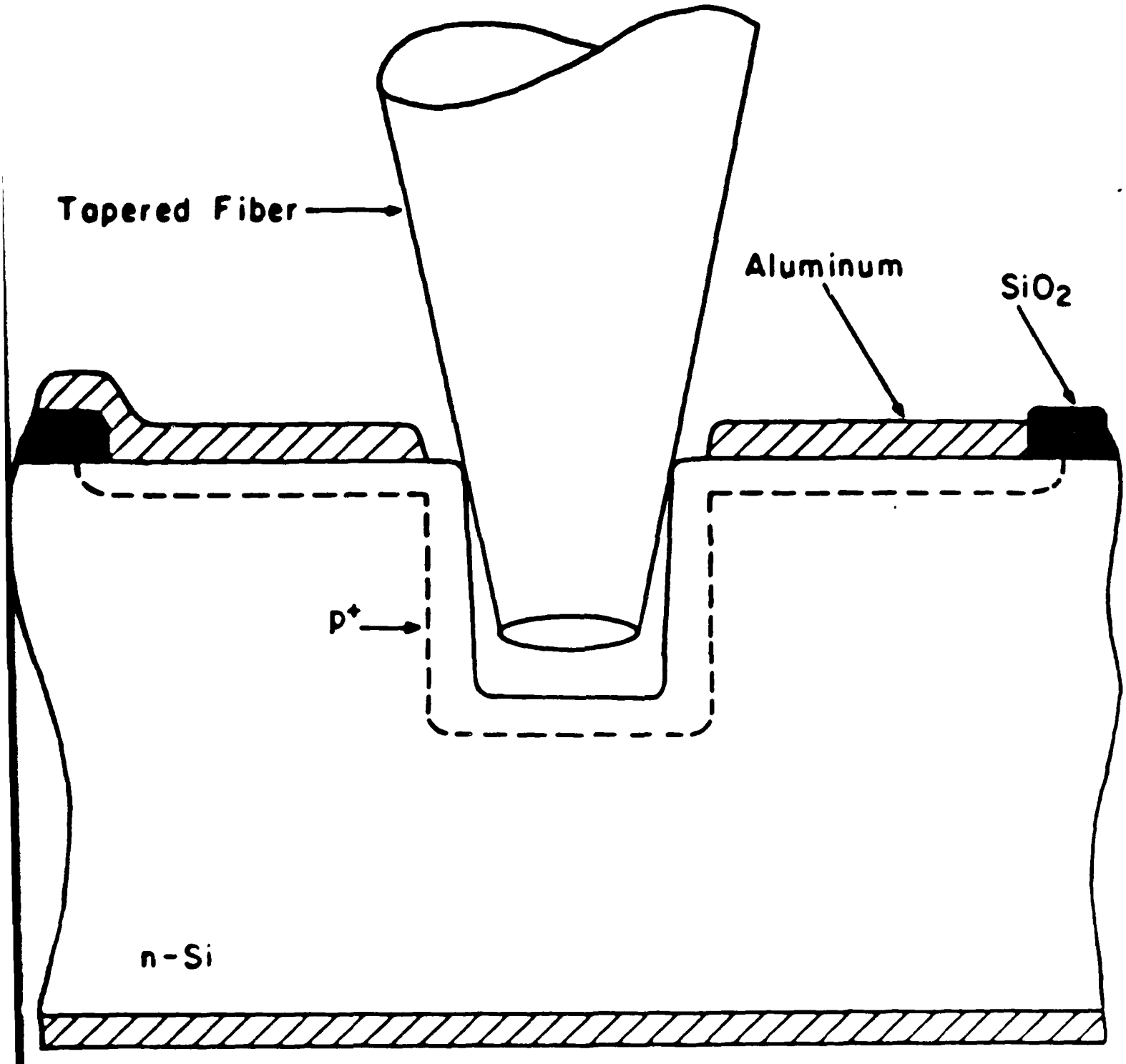

Figure 1. Cross-section of prototype front-side silicon detector IFOC structure.

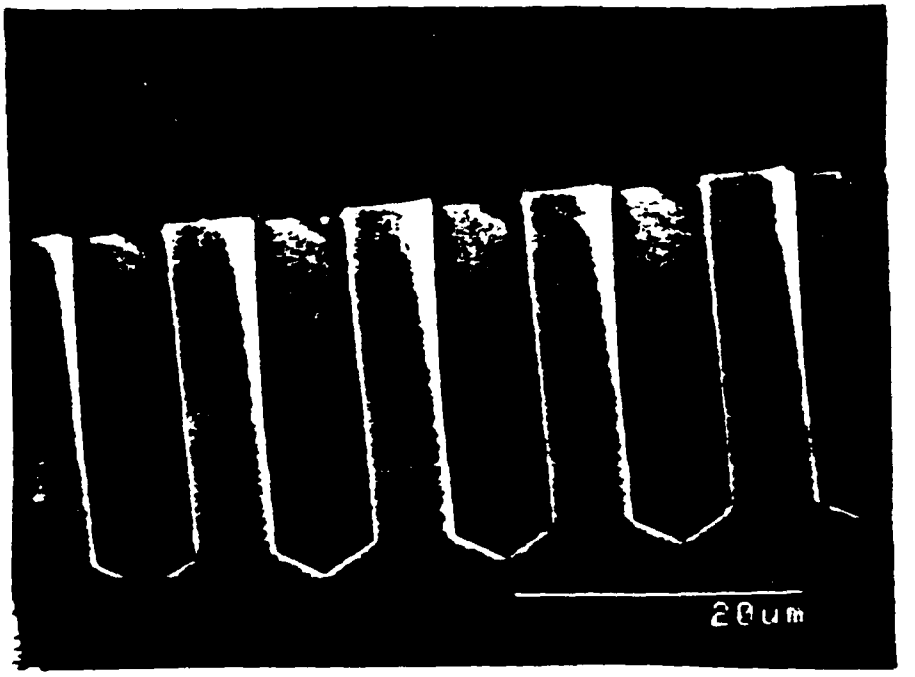

Figure 2(a). SEM cross-section of trenches etched in (110) silicon.

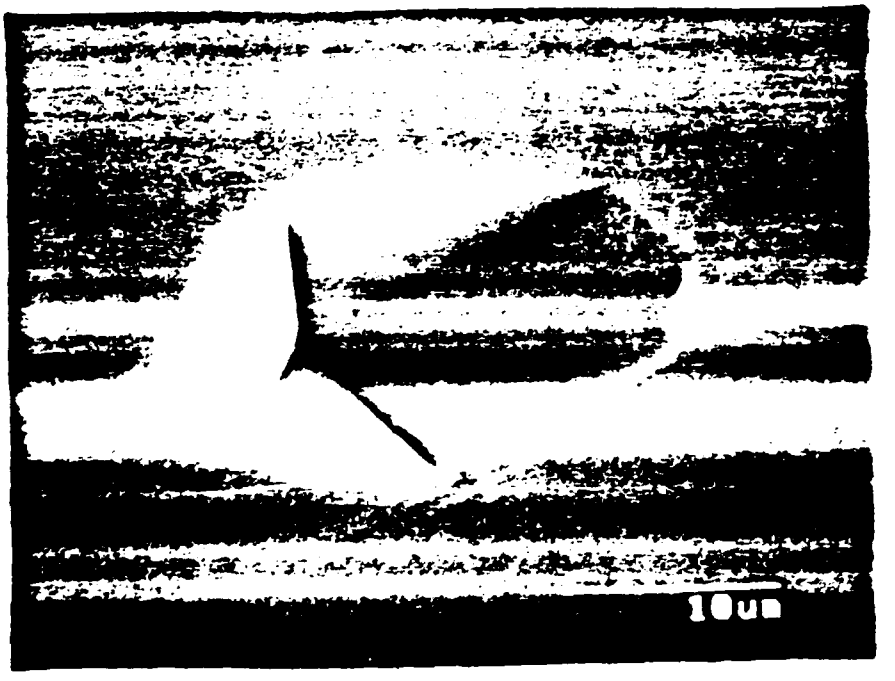

Figure 2(b). SEM cross-section of etched cavity showing two walls perpendicular to the surface. Emerging from the upper right hand corner is (111) plane, which limits depth.

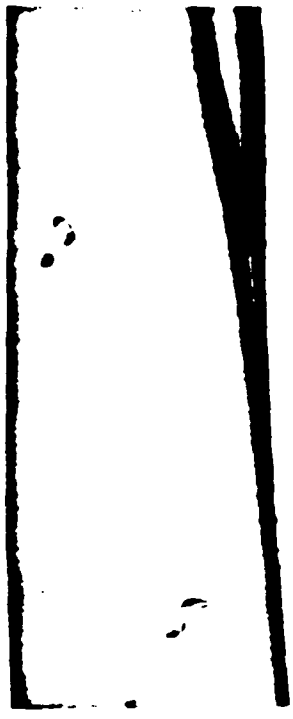

Figure 3(a). Photograph of fiber profile obtained by heating and stretching.

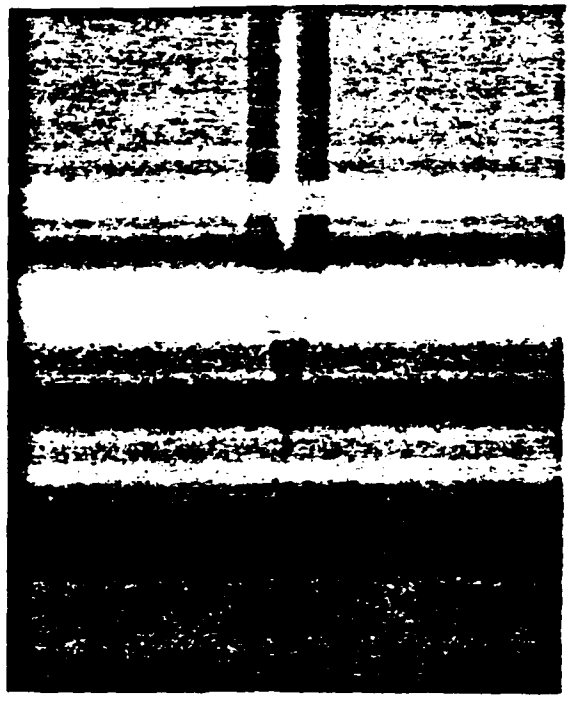

Figure 3(b). Photograph of etched fiber with conical termination.

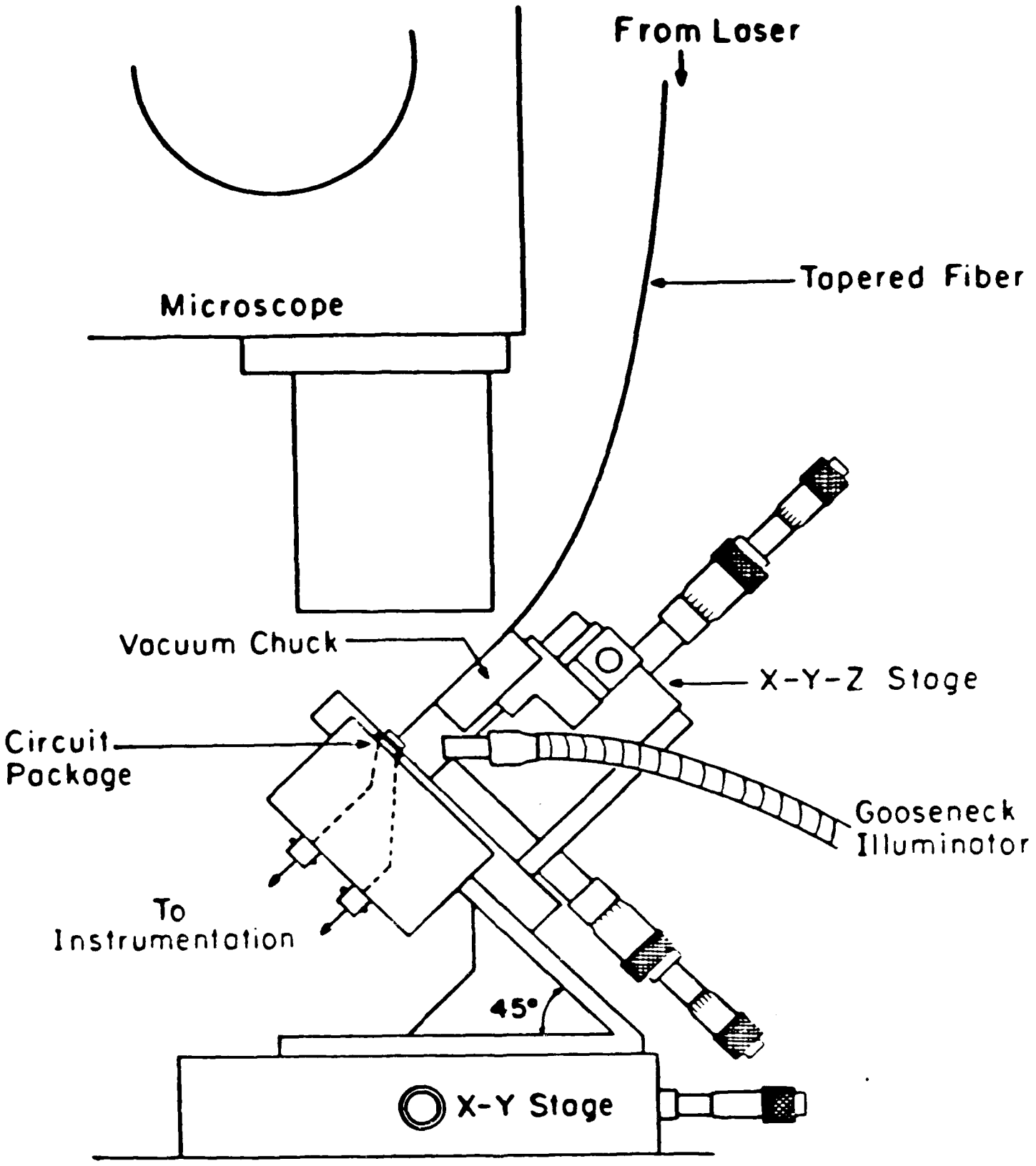

Figure 4. Schematic drawing of the work station used to insert optical fibers into the IFOC cavity.

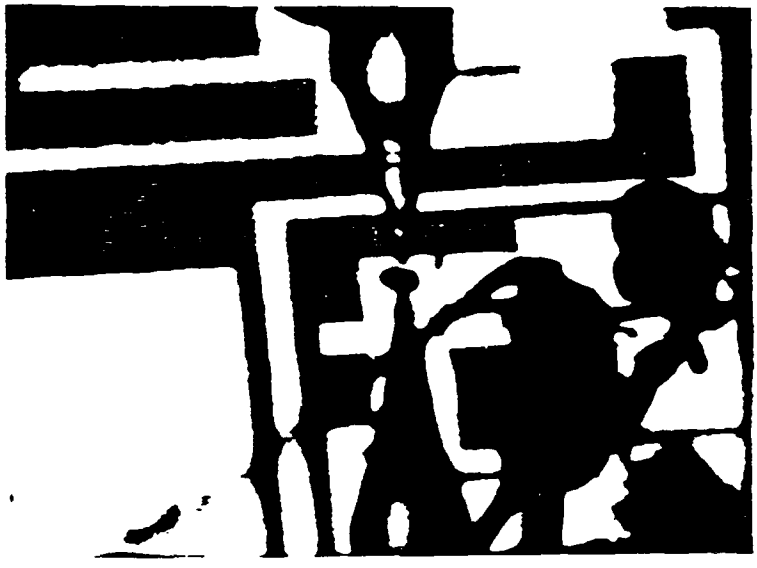

Figure 5(a). Tapered optical fiber about to be inserted into IFOC cavity.

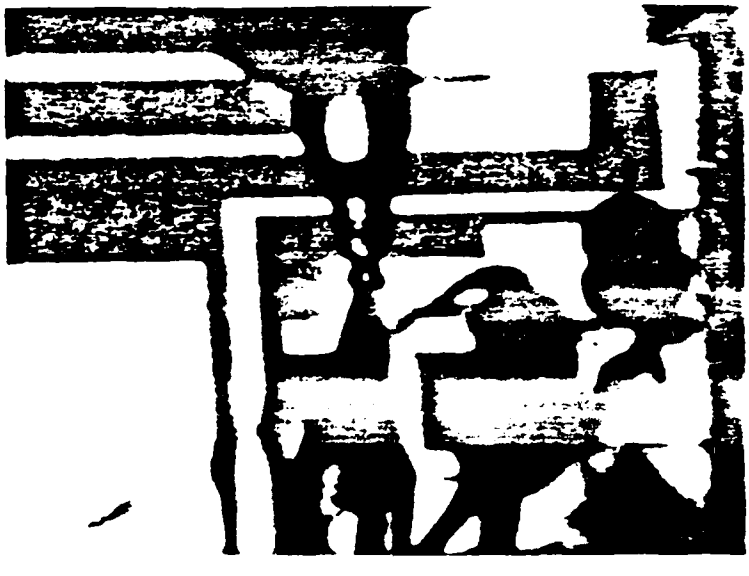

Figure 5(b). Fiber seated in cavity.

Note conventional wire bonds to detector pads used in monitoring photocurrent during insertion process. Fiber image is reflected from surface in both pictures.

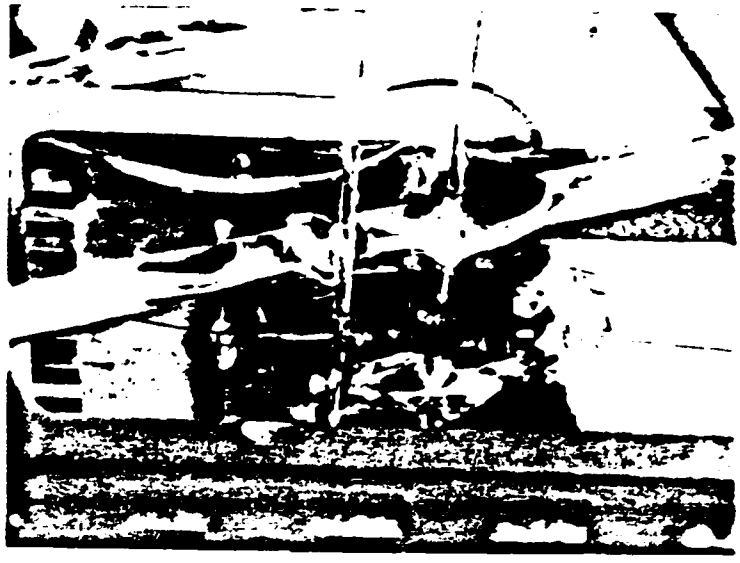

Figure 6. Photograph of packaged device accommodating two IFOC inputs to the interior of IC chip.

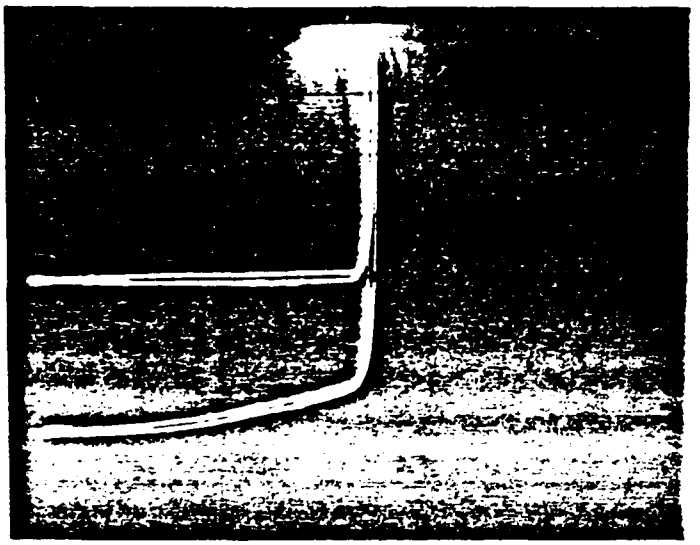

Figure 7. Photograph of dark and illuminated I-V characteristics used to determine net DC responsivity. Horizontal and vertical axes represent 1V and 1uA per division, respectively, and the input optical power is 9uW. Hysteresis is due to capacitance in the external leads of the curve tracer.

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